Exhibit 5

United States Patent [19]

Hynecek

[11] **4,455,739**

[45] **Jun. 26, 1984**

[54] **PROCESS PROTECTION FOR INDIVIDUAL DEVICE GATES ON LARGE AREA MIS DEVICES**

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[21] Appl. No.: **365,077**

[22] Filed: **Apr. 19, 1982**

[51] **Int. Cl.**[3] **H01L 21/90**

[52] **U.S. Cl.** ..... **29/571**; 29/577 C; 29/580

[58] **Field of Search** ..... 29/571, 577 R, 577 C, 29/589, 590, 591, 580; 357/22, 68, 51

[56] **References Cited**

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Attorney, Agent, or Firm—Melvin Sharp; James T. Comfort; David V. Carlson

[57] **ABSTRACT**

Gates of individual devices on a slice are connected through a resistance to the device substrate, and through the same resistance to other device gates. This interconnection and high-resistance drain gives the gate protection from static charge buildup and subsequent catastrophic discharge which would result in a faulty device. This method protects each gate from the time of deposition to final device packaging.

18 Claims, 4 Drawing Figures

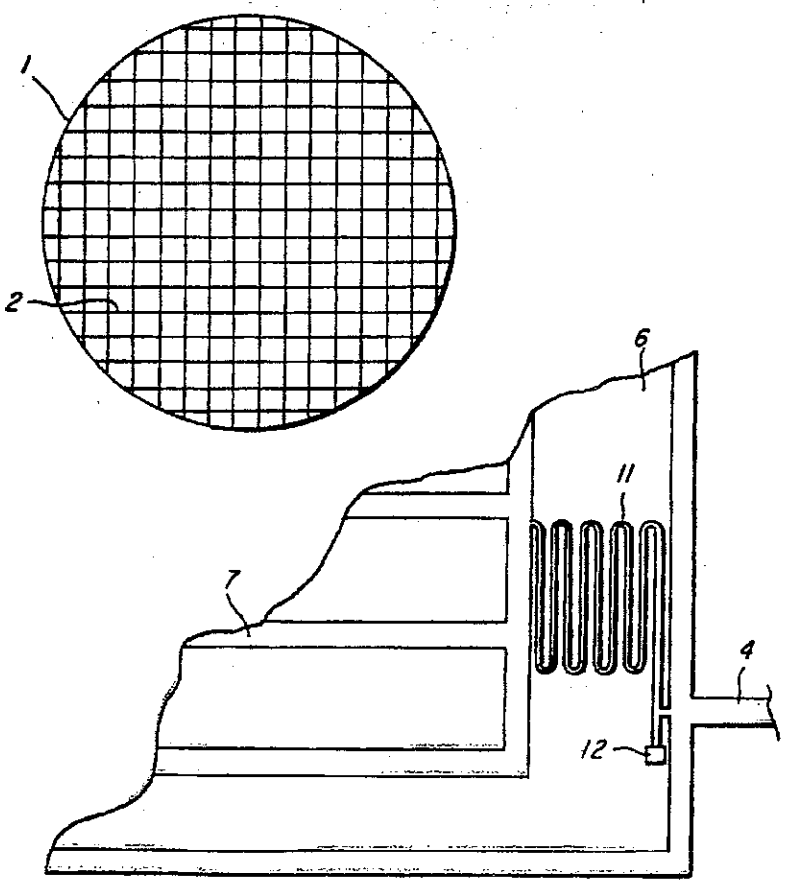


Fig. 1

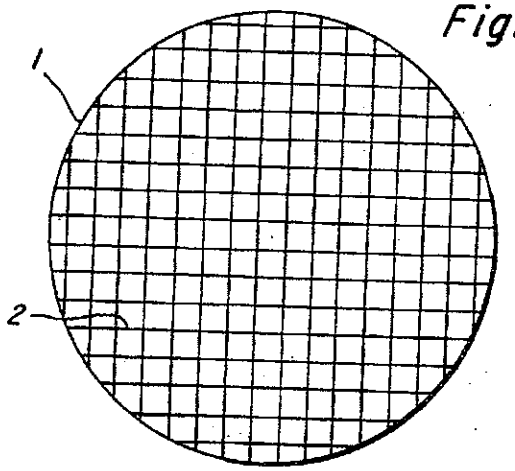
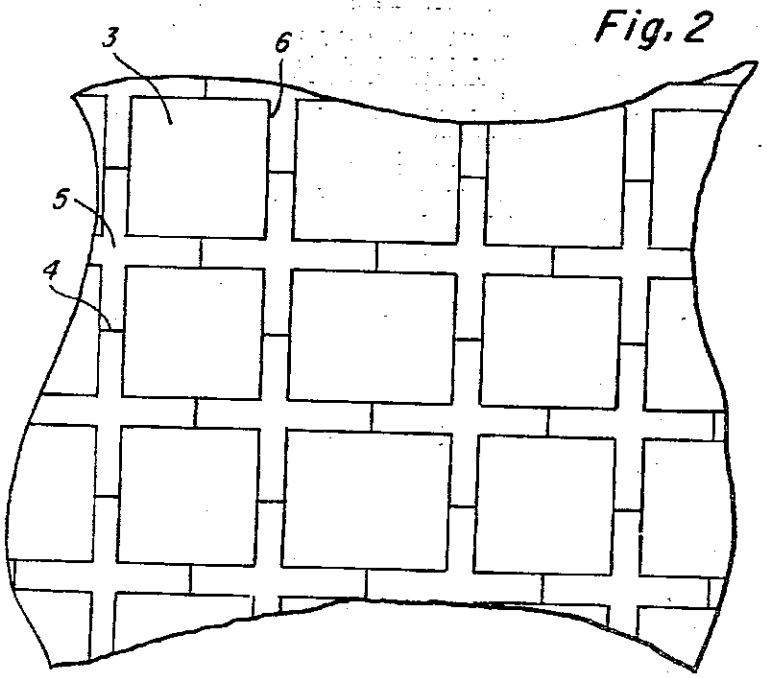


Fig. 2



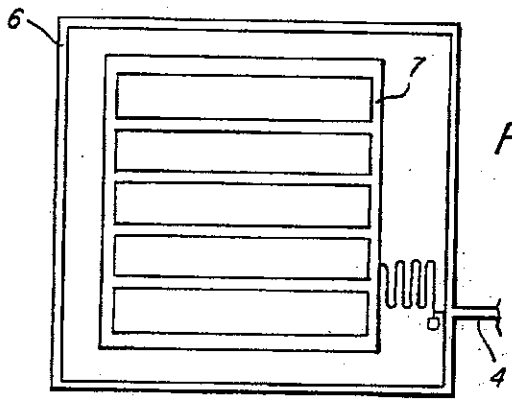
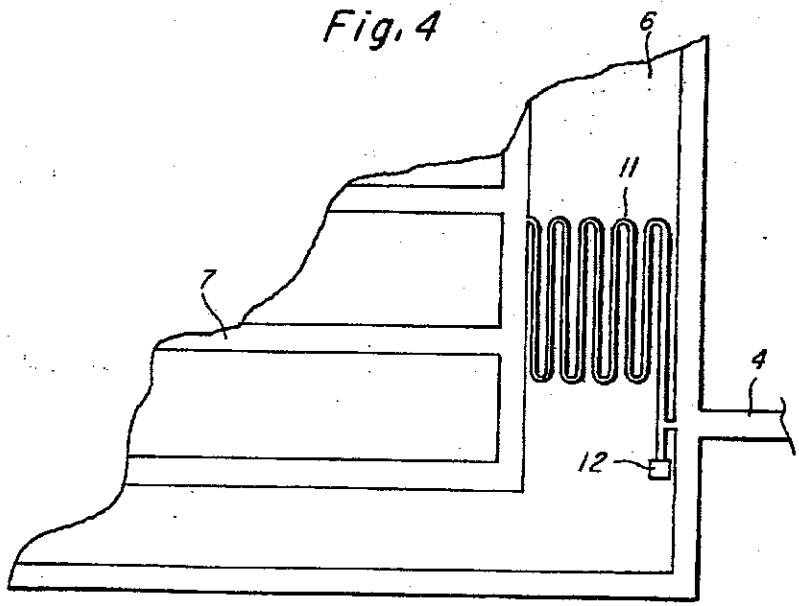


Fig. 3

Fig. 4



PROCESS PROTECTION FOR INDIVIDUAL DEVICE GATES ON LARGE AREA MIS DEVICES

BACKGROUND OF THE INVENTION

This invention relates to yield improvement in semiconductor device and more specifically to protection of individual device gates on large area metal-insulator-semiconductor devices during all stages of processing.

For purposes of this disclosure, a metal-insulator-semiconductor device denotes a device which has a gate separated from a semiconductor by an insulator. The gate is typically metal, but may be of other material, such as polysilicon.

Large area MIS arrays, such as virtual phase charge-coupled device arrays, are susceptible to static charge buildup and subsequent catastrophic discharge during various phases of the fabrication process. The static discharge can be of sufficient energy to damage, or even destroy, the dielectric layer between the gate and the corresponding opposite electrode, if the breakdown point of the material in the layer is reached or exceeded.

This build-up of static charge is unavoidable since the large area device gate structure acts as a capacitor. The large capacitance represented by the gate can store enough energy to cause the damage to the dielectric layer described above. When the accumulated potential reaches or exceeds the breakdown point of the dielectric, the discharge usually occurs in a localized area, typically the weakest point in the dielectric layer. The discharge of this energy through a small point in the dielectric causes structural damage to the dielectric which is not repairable. The result of this damage is a shorted gate or large dark current spot and therefore, a defective device.

An example of a typical operation which would cause the static build-up is the ion-implantation process. A typical dosage of an implant may cause charging of the gate, relative to the substrate, to a field strength exceeding the dielectric strength of the dielectric layer.

Prior to the present invention, gate protection from static charge build-up was typically confined to the process steps coming after the metallization step which connected the gates to protection devices such resistors or diodes, usually through metal bus lines.

It is therefore an object of this invention to provide at the time of gate formation, a structure which has a feature that will bleed off the harmful energy build-up or discharge it through an already damaged area on the edge of the slice or where contact is made to the holder, during ion implantation or other process steps.

SUMMARY OF THE INVENTION

In a typical fabrication process, such as disclosed in U.S. Pat. No. 3,914,127, hereby incorporated by reference, a semiconductor slice is divided into a large number of individual units that are regularly spaced from each other and also completely separated by the scribe line, or some other border area for later use in a dicing operation.

On such a slice as described, if no protection is incorporated, each large device will develop at least one discharge-caused defect, and therefore all devices will be useless. However, in the present invention all device gates are interconnected across the scribe lines to form a "super gate," and the breakdown/discharge will occur only in one or a few devices.

In addition to the gate interconnection, among the devices an essential part of the protection is the connection of the gate of each individual device to ground or some reference point through a large value resistor. This connection is made by metallization at an appropriate time in the process prior to dicing of the slice into individual devices. This resistive path from gate to ground or other reference allows charge build-up to be drained off, thereby also protecting the gate during the possible charge build-up caused by the dicing process or subsequent steps performed on individual units. The amount of resistance in the resistive element will be determined largely by the device application. Generally, the resistance should be large enough so as to not interfere with normal circuit operation in the intended application.

The method described here thus provides complete gate protection from deposition all the way to device packaging.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a drawing of a typical semiconductor slice as it appears during the manufacturing process.

FIG. 2 is an enlarged view of part of the slice of FIG. 1.

FIG. 3 is a simplified drawing of one of the devices which make up the slice as shown in FIG. 1.

FIG. 4 is an enlarged drawing of the device in FIG. 3 showing more detail.

DETAILED DESCRIPTION OF THE INVENTION

In FIG. 1, there is shown a typical semiconductor slice as it appears before being scribed to divide the surface into areas on which devices have been constructed. The scribe lines 2 will separate the surface of the slice 1 into individual device islands.

The magnification of the surface of the slice of FIG. 1 is shown in part in FIG. 2. Each square 3 represents a device island, separated from each other by the scribe line area 5. Each device is surrounded by a border area 6, which is connected across the scribe line area 5 by an interconnect 4 to the border area of the devices adjacent to it. The border area 6 and the interconnection 4 are fabricated at the same time in the process as the gate.

FIG. 3 is a simplified drawing of a large area MIS device, showing the gate interconnect 4, border area 6, and gate 7.

A magnified view of the device in FIG. 3 is depicted in FIG. 4. The resistance element 11 is connected to ground or a reference, usually the device substrate, through a metallization contact 12. Prior to the metallization step when the contact is made between the resistor and the reference, the resistor serves as a connection from the gate 7 to the border area 6. With the interconnect strip 4 in place, device to device interconnection on the slice is accomplished. After the metallization interconnect 12 has been formed in the metallization step, which occurs prior to dicing, each gate is then connected to ground or a reference on the device. The slice can then be diced into individual devices without static damage to any individual gate.

A typical resistance for the resistive element 11 is approximately 100 Kohm. However, values may range from a few thousand ohms to a few megohms, depending upon the device application. The minimum resistance value for a device would be just above that value of resistance that would require a power output of the

device that would damage it. An upper limit for the resistance value would be at the point where the resistance is so high it would appear to be an open circuit to the device connected to it, thus providing no protection at all.

The interconnection of gates of all the devices on a slice has the advantage that the protection of all the gates from static charge build-up and resultant discharge through, and break down of, the dielectric is established at the time of gate formation and is maintained all the way through subsequent device processing. This results in a much higher yield of devices from a slice than might otherwise be possible.

The continuous gate protection during device fabrication as described herein is a significant advance in the art of fabrication of large-area MIS devices. While modification and variations of this invention may be attempted, it is intended they be included in the spirit and scope of this invention.

I claim:

1. A method for protecting individual device gates on a semiconductor slice during the device fabrication process, comprising:

interconnecting the gates of a plurality of said individual devices on said slice; and

coupling said interconnected gates to a reference voltage through a resistive element such that charge can flow to and from the gates prior to dicing the slice into individual devices; and

dicing the slice into individual devices.

2. A method for protecting individual device gates on a semiconductor slice during the device fabrication process comprising:

interconnecting the gates of all said individual devices on said slice, each individual device having a border region, wherein said interconnection comprises a strip of material between the border region of individual devices, said border region of individual devices connected to the individual device gate through an individual resistive element, said border region, said resistive element, said gate, and said interconnecting strip all comprising the same material and deposited simultaneously; and

coupling said interconnected gates to a reference voltage through said resistive element.

3. A method as in claim 1, wherein said resistive element is coupled to the substrate of said device.

4. A method for protecting individual device gates on a semiconductor slice during the fabrication process comprising the step of interconnecting the gates of a plurality of individual devices on said slice through individual resistive elements of said individual devices wherein the resistive elements, gates and interconnection material between the gates are comprised of the same material.

5. A method for protecting individual device gates on a semiconductor slice during the device fabrication process, comprising the step of interconnecting the gates of all individual devices, each device having a border region, on said slice through individual resistive elements on said individual devices wherein said interconnection comprises a strip of material between the border region of individual devices said border region of individual devices connected to the individual device gate through said resistive element, said border region, said resistive element, said gate and said interconnecting strip all comprising the same material and deposited simultaneously.

6. The method according to claim 1 wherein the resistance value is 100 Kohms.

7. The method according to claim 4 wherein the resistance value is 100 Kohms.

8. The method according to claim 1 wherein a metalization step occurs after said coupling.

9. The method according to claim 1 wherein an ion implant occurs after said interconnecting step.

10. The method according to claim 1 wherein the interconnection material, gate material and resistive element are all comprised of the same material.

11. The method according to claim 1 wherein the reference voltage is ground.

12. The method according to claim 1 wherein all electrical connections between the gates and the reference voltage are ohmic.

13. The method according to claim 1 wherein the device is a metal-insulator-semiconductor type device.

14. The method according to claim 1 wherein the value of said resistive element is such that charge can flow through at a rate sufficient to prevent the damage to the device.

15. The method according to claim 1 wherein the resistive element remains connected to said device gates after the dicing step and further includes a contact for connecting the individual devices to a reference voltage through said resistive element which is an individual resistive element for each gate.

16. The method according to claim 1 further including connecting the resistive element to the device substrate prior to dicing the slice into individual devices.

17. The method according to claim 5 further comprising an ion implant step occuring after said interconnection step.

18. The method according to claim 4 wherein the resistive element remains connected to said individual device gates after the dicing step and further includes a contact for connecting the individual devices to a reference voltage through the resistive element.

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